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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,804	02/12/2004	Masud Beroz	TESSERA 3.0-236 DIV	5837

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LERNER DAVID, LITENBERG, KRUMHOLZ & MENTLIK
600 SOUTH AVENUE WEST
WESTFIELD, NJ 07090

EXAMINER	
QUINTO, KEVIN V	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,804	BEROZ ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/12/04, 10/18/04.* + 3/25/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1 and 3-8 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 5 and 6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 5 and 6 contain the limitation "a semiconductor chip, a semiconductor wafer, a semiconductor chip package having a dielectric element attached to a chip, a circuit board, a dielectric sheet, a circuit panel, a connection component, an interposer, a substrate, and a dielectric substrate." However the "dielectric element" is never properly described in the specification and no examples of the "dielectric element" have been disclosed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3-6, and 8 are rejected under 35 U.S.C. 102(a,b) as being anticipated by Okamoto et al. (JP 59143352 A).

6. In reference to claims 1 and 8, Okamoto et al. (JP 59143352 A, hereinafter referred to as the "Okamoto" reference). Figures 3 and 5 of Okamoto each disclose a microelectronic assembly with a first microelectronic element (1) having a contact bearing face and one or more contacts (8b) provided at the contact bearing face. A second microelectronic element (4) juxtaposed with the first microelectronic element has a first surface including one or more conductive pads (5). One or more conductive masses (8a, 8b) interconnects the contacts (8b) of the first microelectronic element (1) and the conductive pads (5) of the second microelectronic element (4). Each of the conductive masses (8a, 8b) includes a first region (8a) with a first fusible material (copper or nickel or palladium, abstract) having a first melting temperature and a second region (8b) with a second fusible material (gold) having a second melting temperature which is less than the first melting temperature. Copper, nickel, and palladium all have a higher melting point than gold (see CRC Handbook of Chemistry and Physics, 81st edition, p.12-197 to 12-198). A lead (2) extends between and electrically interconnects the first (1) and second (4) microelectronic elements. The lead (2) is made of copper, a

known flexible material (Ley, USPN 6,362,522 B1, column 3, lines 63-65). It is understood that a plurality or array of leads is formed which extend between and electrically interconnect the first (1) and second (4) microelectronic elements.

7. In reference to claim 3, the first region (8a) of the conductive mass includes a conductive bump (8a, 8b) attached to one of the contacts (8a) of the first microelectronic element (1).

8. With regard to claim 4, the second region (8b) of the conductive mass includes a layer (8b) of fusible conductive material interposed between one of the conductive bumps of the first microelectronic element (1) and one of the conductive pads (5) of the second microelectronic element (4).

9. So far as understood in claims 5 and 6, the first microelectronic element (1) is a semiconductor chip package while the second microelectronic element (4) is a semiconductor chip package having a substrate.

10. Claims 1, 2, 5, 6, and 8 are rejected under 35 U.S.C. 102(a,b) as being anticipated by Yamaji (USPN 5,536,973).

11. In reference to claims 1 and 8, Yamaji (USPN 5,536,973) discloses a device which meets the claims. Figure 2 of Yamaji discloses a microelectronic assembly with a first microelectronic element (11) having a contact bearing face and one or more contacts (11a) provided at the contact bearing face. A second microelectronic element (12) juxtaposed with the first microelectronic element has a first surface including one or more conductive pads (12a). One or more conductive masses (11a, 12a, 12b, 13) interconnects the contacts (11a) of the first microelectronic element (11) and the

conductive pads (12a) of the second microelectronic element (12). Each of the conductive masses (11a, 12a, 12b, 13) includes a first region (11a or 12a or 13) with a first fusible material (for 13 - copper or aluminum or gold, column 4, lines 50-54) having a first melting temperature and a second region (12b) with a second fusible material (low-melting point solder, column 4, lines 17-19) having a second melting temperature which is less than the first melting temperature. Yamaji makes it clear that the other materials (11a, 12a, and 13) have a higher melting point than that of the bump (12b) since it is referred to as the low melting point material (column 4, lines 19-23) having a melting point which the reflow temperature must exceed in order to complete the connection process. An array of flexible leads (13) extends between and electrically interconnects the first (11) and second (12) microelectronic elements.

12. In reference to claim 2, Yamaji (USPN 5,536,973) discloses a device which meets the claims. Figure 2 of Yamaji discloses a microelectronic assembly with a first microelectronic element (11) having a contact bearing face and one or more contacts (11a) provided at the contact bearing face. A second microelectronic element (12) juxtaposed with the first microelectronic element has a first surface including one or more conductive pads (12a). One or more conductive masses (11a, 12a, 12b, 13) interconnects the contacts (11a) of the first microelectronic element (11) and the conductive pads (12a) of the second microelectronic element (12). Each of the conductive masses (11a, 12a, 12b, 13) includes a first region (11a or 12a or 13) with a first fusible material (for 13 - copper or aluminum or gold, column 4, lines 50-54) having a first melting temperature and a second region (12b) with a second fusible material

(low-melting point solder, column 4, lines 17-19) having a second melting temperature which is less than the first melting temperature. Yamaji makes it clear that the other materials (11a, 12a, and 13) have a higher melting point than that of the bump (12b) since it is referred to as the low melting point material (column 4, lines 19-23) having a melting point which the reflow temperature must exceed in order to complete the connection process. Substantially s-shaped leads having tip ends are electrically connected to the contacts (11a) of the first microelectronic element (11) while the terminal ends are permanently attached to the conductive pads (12a) of the second microelectronic element (12).

13. So far as understood in claims 5 and 6, the first microelectronic element (11) is a semiconductor chip while the second microelectronic element (12) is a semiconductor chip package having a substrate (12).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto et al. (JP 59143352 A).

16. In reference to claim 2, Okamoto (JP 59143352 A). Figures 3 and 5 of Okamoto each disclose a microelectronic assembly with a first microelectronic element (1) having

a contact bearing face and one or more contacts (8b) provided at the contact bearing face. A second microelectronic element (4) juxtaposed with the first microelectronic element has a first surface including one or more conductive pads (5). One or more conductive masses (8a, 8b) interconnects the contacts (8b) of the first microelectronic element (1) and the conductive pads (5) of the second microelectronic element (4). Each of the conductive masses (8a, 8b) includes a first region (8a) with a first fusible material (copper or nickel or palladium, abstract) having a first melting temperature and a second region (8b) with a second fusible material (gold) having a second melting temperature which is less than the first melting temperature. Copper, nickel, and palladium all have a higher melting point than gold (see CRC Handbook of Chemistry and Physics, 81st edition, p.12-197 to 12-198). The lead (2) has a tip end that is electrically connected to the contact (8b) of the first microelectronic element and a terminal end which is permanently attached to the conductive pads of the second microelectronic element (4). It is understood that a plurality or array of leads is formed which extend between and electrically interconnect the first (1) and second (4) microelectronic elements. The leads (2) are made of copper, a known flexible material (Ley, USPN 6,362,522 B1, column 3, lines 63-65). Okamoto teaches all of the claimed invention except for the s-shape of the leads. Although the Okamoto device does not teach the exact s-shape as that claimed by Applicant:

> Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).
>
> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these

changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

Therefore claim 2 is not patentably distinguishable over the Okamoto reference.

Allowable Subject Matter

17. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

18. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of a microelectronic assembly with the explicit connective materials as disclosed by the applicant which are used to connect a severable wafer assembly to another microelectronic assembly.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 but starting on July 15, 2005, the new fax phone number will be (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800